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Performance Optimization and algorithmic design of a single stage Low Noise Amplifier (LNA) for L- Band applications

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Original Research Article

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Abstract: Low Noise Amplifier (LNA) is generally the first stage in microwave communication system. The quality factor of the receiver is greatly determined by the performance of LNA. Design of a low noise amplifier (LNA) is a very critical as it amplifies the received signal and contributes most of the noise figure of whole receiver. LNA is an integral component of RF receiver and it performs various functions i.e. amplification, noise reduction, Noise Figure reduction, better stabilization and noise immunization. However, design of a LNA requires the trade-off of many important parameters including gain, Noise Figure (NF), stability, power consumption, cost and design complexity. In this paper, we have designed and optimize the performance of a single stage stable LNA through an optimization algorithm. Our optimized single stage LNA circuit provides a gain of 11.78 dB and noise figure of 1.86 dB. These are the most important design parameter of a LNA. In this design, a microwave BJT numbered AT3103 from Avago technologies was used. The simulation and performance optimization was carried out in Agilent design package Advance Design Systems (ADS). This LNA operates at center frequency of 2 GHZ and it can be used in L-Band satellite applications.

Keywords: Low Noise Amplifier, Optimization, Algorithmic, Radio Frequency, Advance Design System, Noise Figure, single stage, multiple stage.

INTRODUCTION

Communication system with higher data rate is increasing and this demand is gaining increased momentum from higher consumer demand [1]. Low-noise amplifiers (LNA) are the building blocks of any wireless communication system. LNA is usually located very close to the receiving antenna to amplify captured weak signal [2].

The design challenge in LNA is to achieve low noise figure (NF) and high gain simultaneously, while maintaining low power consumption [3]. A well designed LNA with high gain will reduce overall noise from subsequent stages of receiver tremendously by Friis formula. However, the inherent noise of LNA itself is injected directly into the system and impact sensitivity negatively. LNA is one of the most power-hungry and area consuming component in wireless receivers [2]. A single stage LNA could rarely meet high gain requirements, however single stage is the least power consuming topology [4, 5].

In this paper, we had designed a low power, moderate gain, matched and stable LNA for L-band applications. This paper is organized as follows: First we start with a discussion on LNA design parameters. It is followed with a discussion on our design optimization algorithm. We conclude the paper with a discussion on the optimized design result for verification and a conclusion.

LNA DESIGN PARAMETERS

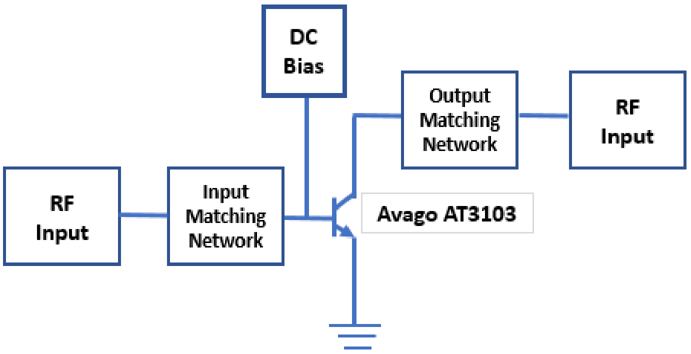

Fig-1: Block representation of a LNA.

Biasing the transistor is the first step in LNA design. We must have to bias the transistor at an operating point that suits our design requirements [2]. The bias point can be selected either for low noise or high gain or high power or low power etc [6]. Biasing network is also responsible for mismatch in source side and load side of LNA. A simplified block diagram that includes DC bias network of a single stage LNA is shown in Fig. 1, where we bias our optimized LNA for a low bias current of 1.63 mA to ensure minimum power, minimum noise and moderate gain.

Stability of a LNA refers to its immunity to spurious oscillations arising from unwanted positive feedback [7]. If we can ensure a very low reverse gain of S_{12}, we can assume the system to be stable and unilateral. LNA's stability can be confirmed by measuring K-factor and $|\Delta|$ factor as in equation (1) and (2).

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{11}S_{22}|} \qquad (1)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \qquad (2)$$

For unconditional stability of a LNA, K>1 and $|\Delta|<1$.

Voltage Standing Wave Ratio (VSWR) on a transmission line is mathematically related to the ratio of reflected power to forward power. If the impedance of the load is not identical to the impedance of the transmission line, the load does not absorb all the RF power and reflection happens. This reflection creates a pattern of voltage peak and voltage valley on the transmission line. VSWR is the ratio of the highest voltage value anywhere along the transmission line to the lowest voltage value [7]. In an ideal system with no reflection VSWR=1.0.

$$VSWR = |V_{max}| / |V_{min}| \qquad (3)$$

where V_{max} is the maximum voltage of the signal along the line, and V_{min} is the minimum voltage along the line. The impedance matching device in a LNA can be a component, circuit, or piece of equipment.

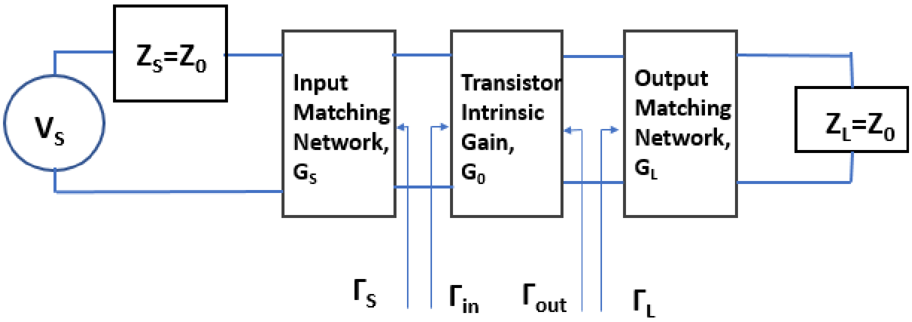

Fig 2: Block diagram of a Single Stage Low Noise Amplifier with input and output matching network.

A block representation of a LNA with matching network and arising reflection co-efficient is shown in Fig. 2. Noise factor, F is a measure of how the signal to noise ratio is degraded by a device. It determines the efficiency, sensitivity and suitability of a LNA for low noise applications. F can be measured from SNR, as shown in equation (4).

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{\frac{S_{in}}{N_{in}}}{\frac{S_{out}}{N_{out}}} \qquad (4)$$

For a receiver that composed of number of stages, each with its own noise figure and gain - noise factor can be determined with Friis formula shown in equation (5).

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_N - 1}{G_1 \ldots G_{N-1}} \qquad (5)$$

which can be simplified for a receiver, having a LNA in the first stage to be:

$$F_{total} = F_{LNA} + \frac{F_{rest} - 1}{G_{LNA}} \qquad (6)$$

MATLAB CODE FOR STABILITY CHECK

```
clc; clear all;
%% stability check
% Data input in polar co-ordinates
as11=162.1; as12=23.7; as21=45.8; as22=-54.6; ms11=0.655; ms12=0.064;
ms21=2.286; ms22=0.569;

% calculation AND data output
[px1,py1]=pol2cart ((pi*(as11+as22))/180, (ms11*ms22));
[px2,py2]=pol2cart (pi*(as12+as21)/180,ms12*ms21);
[THETA_del,RHO_del] = cart2pol((px1-px2),(py1-py2))
aangle=THETA_del*180/3.14
[THETA_deno,RHO_deno]=cart2pol (px2,py2);;
Kfactor=((1-abs(ms11)^2-abs(ms22)^2+abs(RHO_del)^2)/(2*abs(RHO_deno)))

%% Stability Circles---input or source
radius_source= abs(RHO_deno/(abs(ms11)^2-abs(RHO_del)^2))
[a1,b1]=pol2cart ((pi*(as11))/180, (ms11));
[a2,b2]=pol2cart ((pi*(-as22+aangle))/180, (ms22*RHO_del));
at=a1-a2; bt=b1-b2;
c_so_x= at/(abs(ms11)^2-abs(RHO_del)^2);
c_so_y= -bt/(abs(ms11)^2-abs(RHO_del)^2);
[c_the_s,c_rad_s]=cart2pol (c_so_x,c_so_y)
c_angle_source=c_the_s*180/3.14

%% Stability Circles---output or Load
radius_load= abs(RHO_deno/(abs(ms22)^2-abs(RHO_del)^2))
[a3,b3]=pol2cart ((pi*(as22))/180, (ms22));
[a4,b4]=pol2cart ((pi*(-as11+aangle))/180, (ms11*RHO_del));
atL=a3-a4; btL=b3-b4;
c_so_xL= atL/(abs(ms22)^2-abs(RHO_del)^2);
c_so_yL= -btL/(abs(ms22)^2-abs(RHO_del)^2);
[c_the_L,c_rad_L]=cart2pol (c_so_xL,c_so_yL)
c_angle_source=c_the_L*180/3.14
```

where F_{rest} is the overall noise factor of the subsequent stages of a receiver. According to this equation, the LNA can reduce the overall noise figure of the receiver, if it has high gain. Noise figure, NF is the noise factor, expressed in decibels.

$$NF = 10\log(F) = 10\log\left(\frac{SNR_{in}}{SNR_{out}}\right) = SNR_{in,dB} - SNR_{out,dB} \qquad (7).$$

The LNA shown in Fig. 2, having source, Z_s and load impedance, Z_L models the mismatch at input and output. The overall gain for this LNA can be given by:

$$G_T = G_S G_O G_L \qquad (8)$$

where, G_S and G_L are effective gains due to the impedance matching of the transistor at input and output. Fig. 3 shows the possible maximum gain circle of the LNA as well as gain circle movement as matching network are introduced for impedance matching and stability.

DESIGN OPTIMIZATION ALGORITHM

Selection and design of a proper bias circuit is the first step in the design of a LNA. Isolation between RF and DC part of the circuit was achieved by using the RF choke and condensers. In the second step, we synthetize input and output reflection coefficients to ensure the stability, low noise figure and high gain. Last step was the fine tuning and optimization of the lengths of the transmission lines in the matching circuit to minimize the noise figure of the amplifier and maximize the gain. It was done by applying several optimization algorithms until optimal solution is reached and specifications are meet. Some key steps in the design of our LNA are –

Step 1: Selection of S-parameter model of the active device.
Step 2: Inclusion of bias network that is required for the specified S-parameter of interest.
Step 3: Evaluation of stability at design frequency as well as ensuring very low noise figure by minimizing resistance use.
Step 4: Plot of available gain (GA) and noise figure circles, from there we decide the design tradeoff between gain and noise.
Step 5: Design of matching network for allowable VSWR value and plot the VSWR circle.
Step 6: Simulate the design over wide frequency range and ensure that the design is stable over the range.
Step 7: Modify circuit if necessary with frequency-dependent stabilizing circuits.

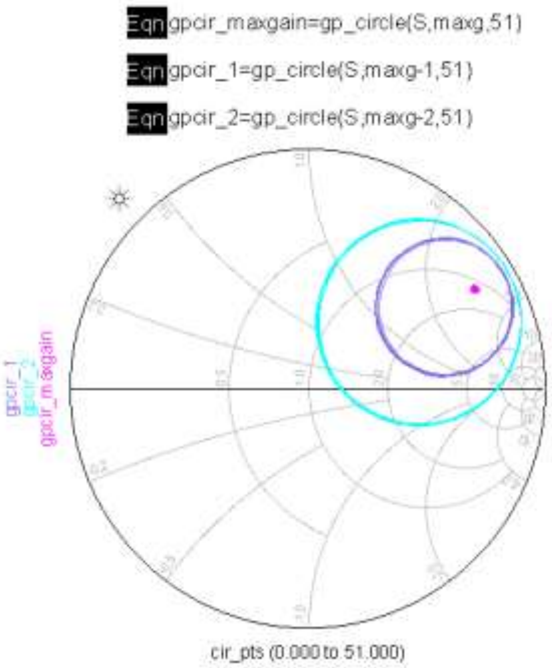

Fig-3: Maximum gain circle simulation of LNA for design contour guidance.

OPTIMIZED SIMULATION RESULTS

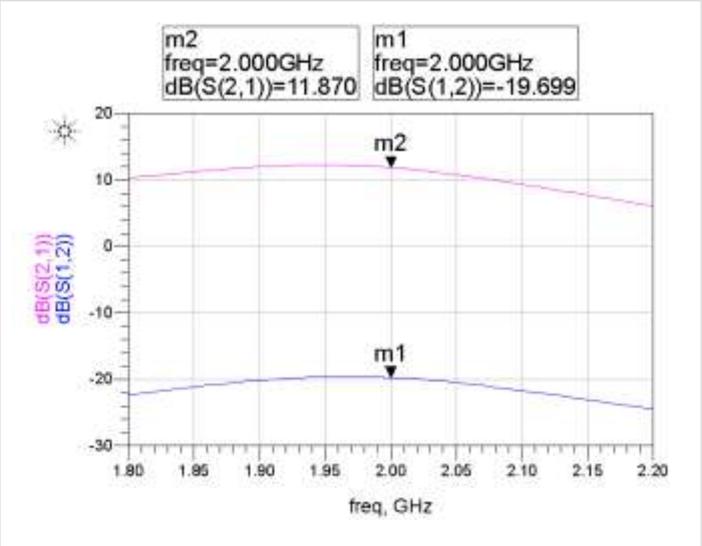

Fig-4: Forward gain and Reverse gain of the LNA.

The simulation result is reported in this section. In Fig. 4, we can see that the forward gain and reverse gain of the optimized LNA to be 11.87 dB and -16.699 dB, respectively. Although in linear scale the forward gain from LNA is nearly 4, and it is enough for the subsequent stages to detect and amplify a very weak RF signal.

We have checked the reflection co-efficient of our design by simulating VSWR from input side and output side as shown in Fig. 5. The input VSWR 2.5 and the output VSWR is 2.001, which are acceptable and within our design specification. The noise figure of the LNA is shown in Fig. 6. The value of Rollett's stability factor simulation confirms the unconditional stability of the Optimized LNA. We had stated in equation (1) and (2) that by ensuring k>1 and Δ<1, we can ensure unconditional stability of our designed LNA.

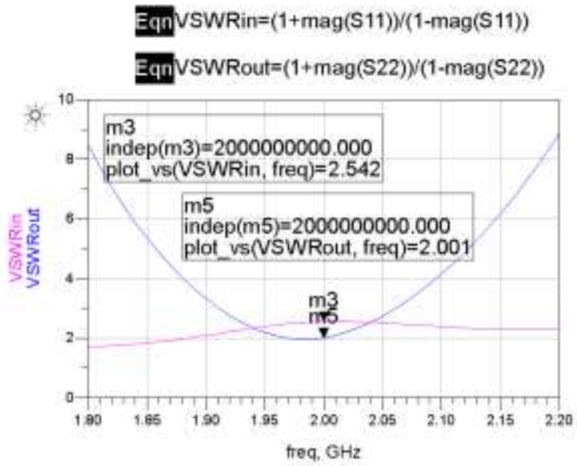

Fig-5: VSWR of the optimized LNA.

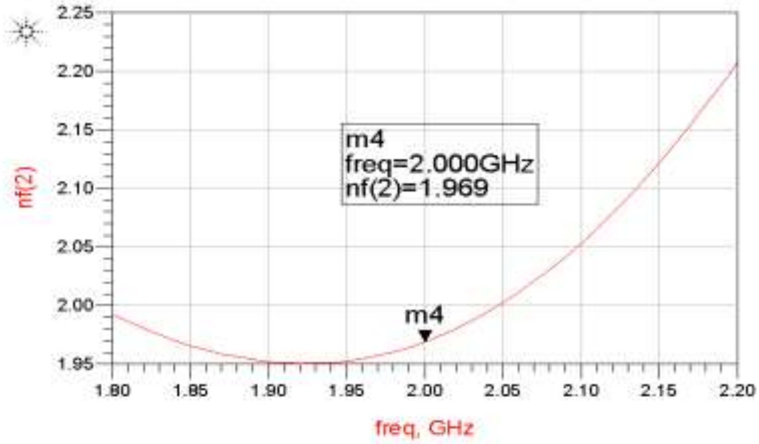

Fig-6: Noise Figure of the designed LNA.

CONCLUSION

A very low power BJT based low noise amplifier (LNA) has been designed and optimized using step by step optimization algorithm. The BJT transistor is biased to operate in Common Emitter configuration. This single stage, low power LNA is suitable for L-Band satellite application with operating frequency of 2GHz. It has a forward gain of 11.87 dB, noise figure of 1.96 dB, reverse gain of -19.69 dB. To ensure low power consumption and to have better mobility operating time, we had biased this LNA with bias current of 1.64mA. The chip area estimate of the LNA from the layout is 7.1347 cm^2 which is equivalent to 983 mil × 1125 mil.

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